AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor device comprising a memory thin film transistor comprising:

a semiconductor active layer over an insulating surface, comprising a channel forming region, a source region and a drain region~~, over an insulating surface~~;

a layer adjacent to the semiconductor active layer with a first insulating film therebetween; and

a control gate electrode adjacent to the layer with a second insulating film therebetween,

wherein the layer adjacent to the semiconductor active layer traps electrons,

wherein the control gate is a laminate film comprising a first film and a second film,

wherein the first film comprises tantalum nitride,

wherein the second film comprises tungsten, and

~~wherein the first film and the second film are formed by sputtering using an inert gas as a sputtering gas.~~

wherein a border of the channel forming region and the drain region is aligned with an edge of the layer.

2.-76. (Canceled)

77. (Currently Amended) A semiconductor device comprising a memory thin film transistor comprising:

a first semiconductor active layer over an insulating surface, comprising a channel forming region, a source region and a drain region~~, over an insulating surface~~;

a floating gate electrode adjacent to the semiconductor active layer with a first insulating film therebetween;

a control gate electrode adjacent to the floating gate electrode with a second insulating film therebetween,

wherein the control gate is a laminate film comprising a first film and a second film,

wherein the first film comprises tantalum nitride,

wherein the second film comprises tungsten, and

~~wherein the first film and the second film are formed by sputtering using an inert gas as a sputtering gas.~~

wherein a border of the channel forming region and the drain region is aligned with an edge of the floating gate.

78. (Currently Amended) A semiconductor device comprising:

a substrate having an insulating surface;

a non-volatile memory over the substrate;

a pixel portion;

a source wiring driver circuit for driving the pixel portion over the substrate;

a gate wiring driver circuit for driving the pixel portion over the substrate; and

wherein the non-volatile memory comprises a memory thin film transistor comprising:

a semiconductor active layer over an insulating surface, comprising a channel forming region, a source region and a drain region~~, over the insulating surface~~;

a layer adjacent to the semiconductor active layer with a first insulating film therebetween; and

a control gate electrode adjacent to the layer with a second insulating film therebetween,

wherein the layer adjacent to the semiconductor active layer traps electrons,

wherein the control gate is a laminate film comprising a first film and a second film,

wherein the first film comprises tantalum nitride,

wherein the second film comprises tungsten, and

~~wherein the first film and the second film are formed by sputtering using an inert gas as a sputtering gas.~~

wherein a border of the channel forming region and the drain region is aligned with an edge of the layer.

79. (Currently Amended) A semiconductor device comprising a non-volatile memory comprising:

an X-address decoder;

a Y-address decoder;

n first signal lines electrically connected to the X-address decoder;

m second signal lines electrically connected to the Y-address decoder;

m third signal lines electrically connected to the Y-address decoder; and

n x m memory thin film transistors arranged in a matrix, each of which comprises:

a semiconductor active layer over an insulating surface, comprising a channel forming region, a source region electrically connected to corresponding one of the m second signal lines, and a drain region electrically connected to corresponding one of the m third signal lines;

a layer adjacent to the semiconductor active layer with a first insulating film therebetween; and

a control gate electrode electrically connected to corresponding one of the n first signal lines, adjacent to the layer with a second insulating film therebetween,

wherein n and m are natural numbers,

wherein the layer adjacent to the semiconductor active layer traps electrons,

wherein the control gate is a laminate film comprising a first film and a second film

wherein the first film comprises tantalum nitride,

wherein the second film comprises tungsten, and

~~wherein the first film and the second film are formed by sputtering using an inert gas as a sputtering gas.~~

wherein a border of the channel forming region and the drain region is aligned with an edge of the layer.

80. (Currently Amended) A semiconductor device comprising a non-volatile memory comprising:

an X-address decoder;

a Y-address decoder;

n first signal lines electrically connected to the X-address decoder;

m second signal lines electrically connected to the Y-address decoder;

m third signal lines electrically connected to the Y-address decoder; and

n x m memory thin film transistors arranged in a matrix, each of which comprises:

a semiconductor active layer over an insulating surface, comprising a channel forming region, a source region electrically connected to corresponding one of the m second signal lines, and a drain region electrically connected to corresponding one of the m third signal lines;

a floating gate electrode adjacent to the semiconductor active layer with a first insulating film therebetween; and

a control gate electrode electrically connected to corresponding one of the n first signal lines, adjacent to the floating gate electrode with a second insulating film therebetween,

wherein n and m are natural numbers,

wherein the control gate is a laminate film comprising a first film and a second film,

wherein the first film comprises tantalum nitride,

wherein the second film comprises tungsten, and

~~wherein the first film and the second film are formed by sputtering using an inert gas as a sputtering gas.~~

wherein a border of the channel forming region and the drain region is aligned with an edge of the floating gate.

81. (Previously Presented) A semiconductor device according to claim 77, wherein the second insulating film comprises an oxide film.

82. (Previously Presented) A semiconductor device according to claim 78, wherein the second insulating film comprises an oxide film.

83. (Previously Presented) A semiconductor device according to claim 79, wherein the second insulating film comprises an oxide film.

84. (Previously Presented) A semiconductor device according to claim 80, wherein the second insulating film comprises an oxide film.

85.-86. (Canceled)

87. (Previously Presented) A semiconductor device according to claim 77, wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

88. (Previously Presented) A semiconductor device according to claim 78, wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

89. (Previously Presented) A semiconductor device according to claim 79, wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

90. (Previously Presented) A semiconductor device according to claim 80, wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

91.-92. (Canceled)

93. (Previously Presented) A semiconductor device according to claim 77, wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

94. (Previously Presented) A semiconductor device according to claim 78, wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

95. (Previously Presented) A semiconductor device according to claim 79,

wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

96. (Previously Presented) A semiconductor device according to claim 80,

wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

97. (Previously Presented) A semiconductor device according to claim 1,

wherein a laminate film further comprises a third film, and

wherein the third film comprises tungsten nitride and an inert element.

98. (Previously Presented) A semiconductor device according to claim 77,

wherein a laminate film further comprises a third film, and

wherein the third film comprises tungsten nitride and an inert element.

99. (Previously Presented) A semiconductor device according to claim 78,

wherein a laminate film further comprises a third film, and

wherein the third film comprises tungsten nitride and an inert element.

100. (Previously Presented) A semiconductor device according to claim 79,

wherein a laminate film further comprises a third film, and

wherein the third film comprises tungsten nitride and an inert element.

101. (Previously Presented) A semiconductor device according to claim 80,

wherein a laminate film further comprises a third film, and

wherein the third film comprises tungsten nitride and an inert element.

102. (Previously Presented) A semiconductor device according to claim 1,

wherein the second insulating film comprises an oxide film.

103. (Previously Presented) A semiconductor device according to claim 1, wherein the layer adjacent to the first semiconductor active layer is an electrically conductive layer.

104. (Canceled)

105. (Previously Presented) A semiconductor device according to claim 78, wherein the layer adjacent to the semiconductor active layer is an electrically conductive layer.

106. (Previously Presented) A semiconductor device according to claim 79, wherein the layer adjacent to the semiconductor active layer is an electrically conductive layer.

107. (Canceled)

108. (Previously Presented) A semiconductor device according to claim 1, wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

109. (Previously Presented) A semiconductor device according to claim 1, wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

110. (Previously Presented) A semiconductor device according to claim 1, wherein the inert element is xenon.

111. (Previously Presented) A semiconductor device according to claim 77, wherein the inert element is xenon.

112. (Previously Presented) A semiconductor device according to claim 78, wherein the inert element is xenon.

113. (Previously Presented) A semiconductor device according to claim 79, wherein the inert element is xenon.

114. (Previously Presented) A semiconductor device according to claim 80, wherein the inert element is xenon.

115. (Previously Presented) A semiconductor device according to claim 77, wherein the floating gate comprises silicon to which one conductivity is imparted.

116. (Previously Presented) A semiconductor device according to claim 80, wherein the floating gate comprises silicon to which one conductivity is imparted.

117. (Previously Presented) A semiconductor device according to claim 1, further comprising:

a switching thin film transistor comprising:

a second semiconductor active layer over the insulating surface; and

a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween,

wherein the semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island, and

wherein a first thickness of the semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer.

118. (Previously Presented) A semiconductor device according to claim 77, further comprising:

a switching thin film transistor comprising:

a second semiconductor active layer over the insulating surface; and

a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween,

wherein the semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island, and

wherein a first thickness of the semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer.

119. (Previously Presented) A semiconductor device according to claim 78,

wherein the non-volatile memory further comprises:

a switching thin film transistor comprising:

a second semiconductor active layer over the insulating surface; and

a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween,

wherein the semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island, and

wherein a first thickness of the semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer.

120. (Previously Presented) A semiconductor device according to claim 79,

wherein the non-volatile memory further comprises:

n x m switching thin film transistors, each of which comprising:

a second semiconductor active layer over the insulating surface; and

a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween,

wherein the semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island, and

wherein a first thickness of the semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer.

121. (Previously Presented) A semiconductor device according to claim 80,

wherein the non-volatile memory further comprises:

n x m switching thin film transistors, each of which comprising:

a second semiconductor active layer over the insulating surface; and

a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween,

wherein the semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island, and

wherein a first thickness of the semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer.

122. (Currently Amended) A semiconductor device comprising a memory thin film transistor comprising:

a semiconductor active layer comprising a channel forming region, a source region and a drain region;

a layer adjacent to the semiconductor active layer with a first insulating film therebetween; and

a control gate electrode adjacent to the layer with a second insulating film therebetween,

wherein the layer adjacent to the semiconductor active layer traps electrons,

wherein the control gate is a laminate film comprising a first film and a second film,

wherein the first film comprises tantalum nitride,

wherein the second film comprises tungsten, and

~~wherein the first film and the second film are formed by sputtering using an inert gas as a sputtering gas.~~

wherein a border of the channel forming region and the drain region is aligned with an edge of the layer.

123. (Currently Amended) A semiconductor device comprising a memory thin film transistor comprising:

a semiconductor active layer comprising a channel forming region, a source region and a drain region;

a floating gate electrode adjacent to the semiconductor active layer with a first insulating film therebetween;

a control gate electrode adjacent to the floating gate electrode with a second insulating film therebetween,

wherein the control gate is a laminate film comprising a first film and a second film,

wherein the first film comprises tantalum nitride,

wherein the second film comprises tungsten, and

~~wherein the first film and the second film are formed by sputtering using an inert gas as a sputtering gas.~~

wherein a border of the channel forming region and the drain region is aligned with an edge of the floating gate.

124. (Currently Amended) A semiconductor device comprising a non-volatile memory comprising:

an X-address decoder;

a Y-address decoder;

n first signal lines electrically connected to the X-address decoder;

m second signal lines electrically connected to the Y-address decoder;

m third signal lines electrically connected to the Y-address decoder; and

n x m memory thin film transistors arranged in a matrix, each of which comprises:

a semiconductor active layer comprising a channel forming region, a source region electrically connected to corresponding one of the m second signal lines, and a drain region electrically connected to corresponding one of the m third signal lines;

a layer adjacent to the semiconductor active layer with a first insulating film therebetween; and

a control gate electrode electrically connected to corresponding one of the n first signal lines, adjacent to the layer with a second insulating film therebetween,

wherein n and m are natural numbers,

wherein the layer adjacent to the semiconductor active layer traps electrons,

wherein the control gate is a laminate film comprising a first film and a second film,

wherein the first film comprises tantalum nitride,

wherein the second film comprises tungsten, and

~~wherein the first film and the second film are formed by sputtering using an inert gas as a sputtering gas.~~

wherein a border of the channel forming region and the drain region is aligned with an edge of the layer.

125. (Currently Amended) A semiconductor device comprising a non-volatile memory comprising:

an X-address decoder;

a Y-address decoder;

n first signal lines electrically connected to the X-address decoder;

m second signal lines electrically connected to the Y-address decoder;

m third signal lines electrically connected to the Y-address decoder; and

n x m memory thin film transistors arranged in a matrix, each of which comprises:

a semiconductor active layer comprising a channel forming region, a source region electrically connected to corresponding one of the m second signal lines, and a drain region electrically connected to corresponding one of the m third signal lines;

a floating gate electrode adjacent to the semiconductor active layer with a first insulating film therebetween; and

a control gate electrode electrically connected to corresponding one of the n first signal lines, adjacent to the floating gate electrode with a second insulating film therebetween,

wherein n and m are natural numbers,

wherein the control gate is a laminate film comprising a first film and a second film,

wherein the first film comprises tantalum nitride,

wherein the second film comprises tungsten, and

~~wherein the first film and the second film are formed by sputtering using an inert gas as a sputtering gas.~~

wherein a border of the channel forming region and the drain region is aligned with an edge of the floating gate.

126. (Previously Presented) A semiconductor device according to claim 122, wherein the second insulating film comprises an oxide film.

127. (Previously Presented) A semiconductor device according to claim 123, wherein the second insulating film comprises an oxide film.

128. (Previously Presented) A semiconductor device according to claim 124, wherein the second insulating film comprises an oxide film.

129. (Previously Presented) A semiconductor device according to claim 125, wherein the second insulating film comprises an oxide film.

130. (Previously Presented) A semiconductor device according to claim 122, wherein a laminate film further comprises a third film, and
wherein the third film comprises tungsten nitride and an inert element.

131. (Previously Presented) A semiconductor device according to claim 123, wherein a laminate film further comprises a third film, and
wherein the third film comprises tungsten nitride and an inert element.

132. (Previously Presented) A semiconductor device according to claim 124, wherein a laminate film further comprises a third film, and
wherein the third film comprises tungsten nitride and an inert element.

133. (Previously Presented) A semiconductor device according to claim 125, wherein a laminate film further comprises a third film, and
wherein the third film comprises tungsten nitride and an inert element.

134. (Previously Presented) A semiconductor device according to claim 122, wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

135. (Previously Presented) A semiconductor device according to claim 123, wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

136. (Previously Presented) A semiconductor device according to claim 124,

wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

137. (Previously Presented) A semiconductor device according to claim 125,

wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

138. (Previously Presented) A semiconductor device according to claim 122,

wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

139. (Previously Presented) A semiconductor device according to claim 123,

wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

140. (Previously Presented) A semiconductor device according to claim 124,

wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

141. (Previously Presented) A semiconductor device according to claim 125,

wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

142. (Previously Presented) A semiconductor device according to claim 122, wherein the layer adjacent to the semiconductor active layer is an electrically conductive layer.

143. (Previously Presented) A semiconductor device according to claim 124, wherein the layer adjacent to the semiconductor active layer is an electrically conductive layer.

144. (Previously Presented) A semiconductor device according to claim 122, wherein the inert element is xenon.

145. (Previously Presented) A semiconductor device according to claim 123, wherein the inert element is xenon.

146. (Previously Presented) A semiconductor device according to claim 124, wherein the inert element is xenon.

147. (Previously Presented) A semiconductor device according to claim 125, wherein the inert element is xenon.

148. (Previously Presented) A semiconductor device according to claim 123, wherein the floating gate comprises silicon to which one conductivity is imparted.

149. (Previously Presented) A semiconductor device according to claim 125, wherein the floating gate comprises silicon to which one conductivity is imparted.

150. (Previously Presented) A semiconductor device according to claim 122, further comprising:

a switching thin film transistor comprising:

a second semiconductor active layer over the insulating surface; and

a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween,

wherein the semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island, and

wherein a first thickness of the semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer.

151. (Previously Presented) A semiconductor device according to claim 123, further comprising:

a switching thin film transistor comprising:

a second semiconductor active layer over the insulating surface; and

a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween,

wherein the semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island, and

wherein a first thickness of the semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer.

152. (Previously Presented) A semiconductor device according to claim 124,

wherein the non-volatile memory further comprises:

n x m switching thin film transistors, each of which comprising:

a second semiconductor active layer over the insulating surface; and

a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween,

wherein the semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island, and

wherein a first thickness of the semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer.

153. (Previously Presented) A semiconductor device according to claim 125,

wherein the non-volatile memory further comprises:

n x m switching thin film transistors, each of which comprising:

a second semiconductor active layer over the insulating surface; and

a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween,

wherein the semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island, and

wherein a first thickness of the semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer.